

Appl. No. 10/829,146
Amdt. Dated April 27, 2005
Reply to Office Action of January 27, 2005

Attorney Docket No. 81751.0071
Customer No.: 26021

REMARKS

This application has been carefully reviewed in light of the Office Action dated January 27, 2005. Claims 1-3 and 5-6 remain in this application. Claims 1 and 5 are the independent Claims. Claims 1-2 and 5-6 have been amended. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Claim Objection

Claims 1 and 5 was objected to because of an informality. In response, applicant added "an" before "inside." It is believed that the substitution addresses the concern of above objection. Reconsideration and withdrawal of the above objection are respectfully requested.

Claim 3 was deemed improper and objected thereto. Applicant respectfully submits the intended objection was directed toward Claim 4, not Claim 3. In response, Claim 4 is canceled, thus rendering this objection moot. Reconsideration and withdrawal of the above objection are respectfully requested.

Art-Based Rejections

Claims 1-6 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 6813532 (Shimoishizaka). Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

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The Shimoishizaka et al. Reference

Shimoishizaka is directed to a semiconductor device having a low elasticity layer disposed on a substrate. According to Shimoishizaka, a metal wire is provided on the low elasticity layer and connected to pads on the substrate. A metal ball connecting to the metal wire is provided. The semiconductor is mounted to a mother board with the metal ball facing the mother board. Accordingly the metal ball functions as an external electrode connecting to a pad on the mother board. (See, Shimoishizaka; Col. 2, lines 52-65; Figures 2 and 9). The stress applied by mounting the semiconductor device to a mother board can be absorbed by the elasticity of the elastic material layer. (See, Shimoishizaka; Col. 2, line 66 - Col. 3, line 7).

The Claims are Patentable Over the Cited References

The present invention is directed to a semiconductor device having an insulating layer formed thereon, the insulating layer including an elastic deformable section.

As defined by amended independent Claim 1, an electronic device including a semiconductor substrate in which an integrated circuit is formed is provided. An insulating layer formed on the semiconductor substrate has a first upper surface. An elastically deformable section forms on the first upper surface. The elastically deformable section forms at a position closer to one of edges of the semiconductor substrate than to a center of the semiconductor substrate. The elastically deformable section has a second upper surface. First and second electrodes are electrically connected with an inside of the semiconductor substrate. The first electrode is formed on the first upper surface. The second electrode is formed on the second upper surface. A first substrate on which a first interconnect pattern is

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formed is provided. The first interconnect pattern faces the first electrode and is electrically connected with the first electrode. A second substrate on which a second interconnect pattern is formed is provided. The second interconnect pattern faces the second electrode and is electrically connected with the second electrode. The elastically deformable section is elastically deformed in a manner to be depressed under the second electrode, and presses the second electrode against the second interconnect pattern due to elasticity.

The applied reference of record fails to teach or suggest the above features of amended independent Claim 1. In particular, Shimoishizaka fails to disclose or suggest, "the elastically deformable section having a second upper surface; first and second electrodes which are electrically connected with an inside of the semiconductor substrate, the first electrode being formed on the first upper surface, the second electrode being formed on the second upper surface" as required by amended independent Claim 1. Moreover, Shimoishizaka fails to disclose or suggest, "a first substrate on which a first interconnect pattern is formed, the first interconnect pattern facing the first electrode and being electrically connected with the first electrode; and a second substrate on which a second interconnect pattern is formed, the second interconnect pattern facing the second electrode and being electrically connected with the second electrode," as required by amended independent Claim 1.

As discussed above, Shimoishizaka is directed to a semiconductor device mounted on a mother board. (See, *Shimoishizaka*; Col. 2, lines 52 - Col. 3, line 1). Shimoishizaka does not disclose or suggest a second upper surface, a second electrode, a second substrate, and a second interconnect pattern. Accordingly, the applied reference cannot be said to teach or suggest features of amended Claim 1. Reconsideration and withdrawal of the rejection are respectfully requested.

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Since the cited reference fails to disclose, teach or suggest the above features recited in amended independent Claims 1, these references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, amended independent Claims 1 is believed to be in condition for allowance and such allowance is respectfully requested.

Independent Claim 5 is allowable for the same foregoing reasons as those discussed in connection with amended independent Claim 1.

The remaining claims depend either directly or indirectly from independent Claims 1 and 5 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are therefore also believed to be in condition for allowance.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

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If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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